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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,610	03/01/2002	Richard A. Nichols	100.152US01	7953

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EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,610	NICHOLS, RICHARD A.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-10,12,13,15-22,24-26,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-10,12,13,15-22,24-26,28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. Objections to the drawings as disclosed in the previous office action are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-2,4-5,7-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin US Patent No.: 6065140) in view of Yamamoto et al (US Patent No.: 6014414).

   a. **Claim 1**, Irwin discloses a phase locked loop comprising a phase comparator (Fig. 3, label 26), a loop filter (Fig. 3, label 38), an oscillator (Fig. 3, label 30), a central processing unit (CPU), inherently containing a machine readable medium used to contain instructions (Fig. 5, label 110), coupled to the oscillator and receiving a status message (Fig. 5, labels 116 and 106). Although Irwin does not explicitly disclose the PLL is placed in holdover when the quality level

of the reference clock signal is below a threshold, Yamamoto et al discloses a synchronization system comprising selecting a reference clock signal, wherein the reference clock signal is a quality control signal, a digital PLL (Fig. 19, label 1912) and a processor (Fig. 19, label 1904), wherein the CPU stores a list of the reference clock signals and controls the selection of the reference clock signal based on the quality levels or failure notifications. (Col. 13, lines 18-67 and Col. 14, lines 1-27). The DPLL uses the reference clock signal to place the DPLL in synchronization, using the reference clock signal as a threshold to register when the system is synchronized. (Col. 2, lines 5-67, Col. 3, lines 1-4, Col. 8, lines 65-67, Col.9, Col. 10, lines 1-28) The DPLL uses a holdover clock signal if switching to a different reference clock fails. Once the DPLL reaches the holdover reference clock signal, the DPLL is placed in holdover until a new reference clock signal is selected. (Col. 11, lines 4-25) It would be obvious to one skilled in the art to incorporate selecting of reference clock signals as disclosed by Yamamoto et al to Irwin's invention to effectively provide synchronized clock signals with highest quality level.

b. **Claim 2**, as explained in claim 1, Yamamoto et al discloses placing the PLL in holdover based on the status message or the reference clock signal. (Col. 8, lines 65-67, Col. 9, Col. 10, lines 1-28 and Col. 11, lines 4-25)

c. **Claim 4** inherits all the limitations of claim 1, but claim 1 does not recite the limitation of selecting a reference clock signal from a group of primary and secondary reference clock signals. Yamamoto et al discloses selecting a

reference clock signal from primary and secondary clock signals. (Col. 2, lines 50-67, Col. 3, lines 1-4 and Col. 10, lines 48-59)

d. **Claim 5** inherits all the limitations of claim 1.

e. **Claim 7**, Yamamoto et al discloses selecting reference clock signal of high quality levels. The quality level of the signals can be at least a stratum 2 level. (Col. 1, lines 66-67 and Col. 2, lines 1-19)

f. **Claim 8** inherits all the limitations of claim 1.

g. **Claim 9** inherits all the limitations of claims 4 and 8.

4. **Claims 10,12-13,15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin US Patent No.: 6065140) in view of Yamamoto et al (US Patent No.: 6014414) and further in view of Dubberly et al (US Patent No.: 5581555).

a. **Claim 10** inherits all the limitations of claim 1, but claim 1 does not recite a receiver, a framer and a prescaler. Dubberly et al discloses a cascaded parallel phase locked loop comprising a receiver (Fig. 8, label 100), a framer (Fig. 8, label 102) and a prescaler coupled between the framer and PLL. (Fig. 14, labels x55 and x389) It would be obvious to one skilled in the art to incorporate a framer and prescaler to Irwin and Yamamoto et al's invention to provide unbunched sequences so to provide easy access to information for synchronization.

b. **Claim 12** inherits all the limitations of claims 1 and 10.

c. **Claim 13** inherits all the limitations of claim 1.

d. **Claim 15** inherits all the limitations of claims 1 and 10.

5. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin US Patent No.: 6065140) in view of Yamamoto et al (US Patent No.: 6014414), further in view of Dubberly et al (US Patent No.: 5581555) and further in view of Baydar et al (US Publication No.: 20020097743).

a. **Claim 16** inherits all the limitations of claim 1 and 10 but claims 1 and 10 does not teach a shelf backplane. Baydar et al discloses a shelf backplane and a plurality of shelf elements coupled to the shelf backplane comprising a synchronization of the plurality of shelf elements (Fig. 6, labels 26 and 28, Fig. 7, labels 26 and 28 and Fig. 8), wherein the timing circuit provides a synchronization timing signal to a shelfplane (Fig. 8, labels 72 and 83 and Fig. 6, labels 26 and 28) and inherently discloses the synchronization timing signal is derived from the first timing signal. (Fig. 8, label 83, page 8, paragraphs [0147][0148][0149], page 9, paragraph [0161] and page 10, paragraph [0164]) It would be obvious to one skilled in the art to allow transmission and reception from other subscribers with different service formats. (page 2, paragraph [0016])

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claim 17,19-22,24-25,30-32** is rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al (US Patent No.: 6014414).

   a. **Claim 17**, Yamamoto et al discloses generating a timing signal from the reference clock signal (Fig. 19, label 1902), monitoring the status message while selecting the reference clock signal (Col. 5, lines 7-12), placing the PLL in holdover if the holdover reference signal is selected (Col. 5, lines 16-24) and such steps of the method are performed in this order (Fig. 19).

   b. **Claim 19**, Yamamoto et al discloses selecting the highest quality level reference clock signal and although Yamamoto et al does not explicitly state such a level is expected, it is possible the selected reference signal is an expected quality level.

   c. **Claim 20**, Yamamoto et al discloses the reference clock signal can have a Stratum level at least 2. (Col. 1, lines 66-67 and Col. 2, lines 1-19)

   d. **Claim 21**, Yamamoto et al discloses placing the PLL in holdover if the holdover signal is selected and the PLL reaches such a level. (Col. 2, lines 5-67, Col. 3, lines 1-4, Col. 8, lines 65-67, Col.9, Col. 10, lines 1-28 and Col. 11, lines 4-25)

   e. **Claim 22** inherits all the limitations of claims 17, but claim 17 does not recite the limitation of selecting the reference clock signal from a primary and secondary reference clock signal. Yamamoto et al discloses selecting a reference clock signal from primary and secondary clock signals. (Col. 2, lines 50-67, Col. 3, lines 1-4 and Col. 10, lines 48-59)

f. **Claim 24**, Yamamoto et al discloses the PLL in holdover until a new reference clock signal is selected. (Col. 2, lines 50-67, Col. 3, lines 1-4 and Col. 10, lines 48-59)

g. **Claim 25**, Although Yamamoto et al does not explicitly state holding the PLL for a predetermined time, the amount of the time it takes to select a new reference clock signal will take a certain amount of time, thus Yamamoto et al inherently discloses placing the PLL in holdover for a predetermined amount of time. (Col. 2, lines 50-67, Col. 3, lines 1-4 and Col. 10, lines 48-59)

h. **Claim 30** inherits all the limitations of claim 17.

i. **Claim 31** inherits all the limitations of claim 21.

j. **Claim 32** inherits all the limitations of claim 22.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 26,28,33-34** are rejected under 35 U.S.C. 102(e) as being anticipated by Ogura (US Patent No.: 6542039).

e. **Claim 26**, Ogura discloses when the quality level of a status message is at or above a target level (Fig. 7, Col. 12, lines 41-64, Col. 13, lines 54-67 and Col. 14, lines 1-7), generating a first error signal (Fig. 1, output from phase error detector), filtering a first error signal (Fig. 1, label 9), generating a timing signal

(Fig. 1, label reproduction clock), deriving a first feedback signal (Fig. 1, label reproduction clock). The process stated above is processed again for a second reference signal (Fig. 1, label reproduction clock signal) if the first reference signal is below a target level (Fig. 7), and the second reference signal is at or above the target level (Fig. 7). If either of the reference clock signals is below the target level, the PLL is placed in holdover (Col. 12, lines 41-67, Col. 13, lines 54-67, and Col. 14, lines 1-6) and a timing signal is generated (Fig. 1, label reproduction clock signal). Although Ogura does not explicitly state the method is preformed in the order presented, Ogura discloses an apparatus performing the limitations and thus, Ogura, inherently, discloses performing the method in such an order.

f. **Claim 28** inherits all the limitations of claim 26.

g. **Claims 33 and 34** inherit all the limitations of claim 26.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Osterberg (US Patent No.: 5881374)

   b. Bruce (US Patent No.: 4430636)

   c. Griswold (US Patent No.: 3769602)

   d. Cappels, Sr. (US Patent No.: 5731843)

   e. Johnson et al (US Patent No.: 4849993)

f. Bortolini et al (US Patent No.: 5473640)

g. Barve (US Patent No.: 6856615)

h. Ogawa (US Patent No.: 5574757).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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